IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

		ATTY. DOCKET NO.: RPS920030151US1
IN RE APPLICATION OF:	§	
	§	
KENNETH DOCKSER	§	EXAMINER: **BRIAN P. JOHNSON**
	§	
SERIAL NO.: **10/699,571**	§	CONFIRMATION NO.: **1590**
	§	
FILED: ***OCTOBER 31, 2003***	§	ART UNIT: **2183**
	§	
FOR: **VECTOR EXECUTION UNIT TO PROCESS A VECTOR INSTRUCTION BY EXECUTING A FIRST OPERATION ON A FIRST SET OF OPERANDS AND A SECOND OPERATION ON A SECOND SET OF OPERANDS**	§	

APPEAL BRIEF UNDER 37 C.F.R. 41.37

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Sir:

This Brief is submitted in support of the Appeal of the Examiner's final rejection of Claims 1, 4, 7-10 and 21-34 in the above-identified application. A Notice of Appeal was filed in this case on January 29, 2009 and received in the United States Patent and Trademark Office on January 29, 2009. A one month extension of time is required to submit this Appeal Brief and is hereby requested. Please charge the fee of $130.00 for the one month extension to **Dillon &Yudell LLP Deposit Account No**. 50-3083. Please charge the fee of $500.00 due under 37 C.F.R. §1.17(c) for filing the brief, as well as any additional required fees, to **Deposit Account No. 50-0563.**

REAL PARTY IN INTEREST

The real party in interest in the present Application is International Business Machines Corporation, the Assignee of the present application as evidenced by the Assignment set forth at reel 014474, frame 0057.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, the Appellants' legal representative, or assignee, which directly affect or would be directly affected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1, 4, 7-10 and 21-34 stand finally rejected by the Examiner as noted in the Final Office Action dated October 29, 2008. The rejection of Claims 1, 4, 7-10 and 21-34 is appealed.

STATUS OF AMENDMENTS

Appellants' Amendment D, filed on July 24, 2008 was entered by the Examiner, as noted in the Final Office Action. No amendments were filed subsequent to the Final Office Action from which this Appeal is taken.

SUMMARY OF THE CLAIMED SUBJECT MATTER

As recited by Appellants' independent Claim 1, Appellants' claimed subject matter provides: [a] microprocessor 100 (see paragraph 0014; FIG. 1), comprising: a vector unit 200 (see paragraph 0017, 0018, 0020, 0021; FIG. 1; FIG. 2) to execute a vector instruction 300 (paragraph 0024, 0030) to perform a first operation on a first set of operands and a second operation on a second set of operands (see paragraph 0032); a vector register file 201 comprising a primary register file 202 and a secondary register file 204 (paragraph 0022; FIG. 2); wherein the vector instruction 300 includes a first register field (306) (see paragraph 0024; FIG. 3) indicative of a first primary register in the primary register file 202 and a first secondary register in the secondary register file 204, a second register field (308) indicative of a second primary register in the primary register file 202 and a second secondary register in the secondary register file 204, and a third register field (310) indicative of a third primary register in the

primary register file 202 and a third secondary register in the secondary register file 204 (paragraph 0026; FIG. 2); and wherein the first set of operands includes a first operand selected from the first primary register or the first secondary register, a second operand selected from the second primary register or the second secondary register, and a third operand selected from the third primary register or the third secondary register (see paragraph 0026, 0030), wherein the selection of the operands occurs at substantially a same time to provide an input of the three operands to the vector unit via the three inputs (paragraph 0026).

Appellants' Claim 4 further provides: wherein the vector unit 200 includes a 3-input primary unit 220 and a 3-input secondary unit 230, wherein the primary unit 220 is configured to perform the first operation on the first set of operands and the 3-input secondary unit 230 is configured to perform the second operation on the second set of operands (paragraphs 0026; FIG. 2).

Appellants' Claim 7 further provides: wherein the first and second operations use at least one operand from the primary register file and at least one operand from the secondary register file (see paragraph 0026).

Appellants' Claim 8 provides: wherein the first and second sets of operands include at least one common operand (paragraph 0029).

Appellants' Claim 9 further provides: wherein the vector register file contains information representing a real portion of a complex number in the primary register file and an imaginary portion of the complex number in the secondary register file (see paragraph 0019).

Appellants' Claim 10 provides: wherein the vector unit is configured to execute a complex computation instruction in which the imaginary portion of the first operand of the first set of operands is multiplied by an imaginary portion of a second operand in the first operation and in which the imaginary portion of the first operand is multiplied by a real portion of the second operand in the second operation (paragraph 0019).

Appellants' Claim 21 further provides: wherein the second set of operands include a first operand selected from the first primary register or the first secondary register, a second operand selected from the second primary register or the second secondary register, and a third operand selected from the third primary register or the third secondary register (paragraph 0026; FIG. 2).

Appellants' Claim 22 provides: wherein the first operation includes multiplying two of the three first set of operands to obtain a first product and adding or subtracting the remaining of the first set of operands to or from the first product and wherein the second operation includes multiplying two of the three second set of operands to obtain a second product and adding or subtracting the remaining of the second set of operands to or from the second product (see paragraph 0027; FIG. 4).

Appellants' Claim 22 also provides: wherein the first and second sets of operands comprise first and second sets of floating point formatted operands (paragraph 0018, 0019, 0026; FIG. 2).

Appellants' Claim 23 provides: wherein the vector instruction includes a target register field indicative of a primary target register in the primary register file and a secondary target register in the secondary register file and further wherein the vector unit is further configured to store a result of the first operation in the primary target register and to store a result of the second operation in the secondary target register (see paragraph 0028; FIG. 2).

Appellants' Claim 25 also provides: [a] vector unit 205 to process a vector instruction 300 having an opcode 302-1, 302-2 and first, second, and third register fields (306, 308, 310) (see FIG. 3) comprising: a register file including a primary register file 202 having a set of primary registers and a secondary register file 204 having a set of secondary registers, wherein each register field identifies a register in the primary register file 202 and a corresponding register in the secondary register file 204 (paragraph 0022, 0026; FIG. 2); primary and secondary calculating units 220/230, wherein the primary calculating unit 220 includes first, second, and third inputs to receive, respectively, first, second, and third operands of a first set of operands and wherein the secondary calculating unit 230 includes

first, second, and third inputs to receive, respectively, first, second, and third operands of a second set of operands (see paragraph 0026; FIG. 2); and multiplexing circuitry (222-236) (paragraph 0024, 0026; FIG. 2) controlled by the opcode to select each of the first, second, and third operands in the first and second set of operands from the set of primary and secondary file registers identified by the register fields (see paragraph 0024, 0026; FIG. 2, FIG. 3).

Appellants' Claim 26 further provides: wherein the multiplexing circuitry is controlled by the opcode to select: the first operand in the first set of operands from either the first primary or the first secondary registers (paragraph 0026; FIG. 2); the second operand in the first set of operands from either the second primary or the second secondary registers (paragraph 0026; FIG. 2); and the third operand in the first set of operands from either the third primary or the third secondary registers (paragraph 0026; FIG. 2); the first operand in the second set of operands from either the first primary or the first secondary registers (paragraph 0026; FIG. 2); the second operand in the second set of operands from either the second primary or the second secondary registers (paragraph 0026; FIG. 2); and the third operand in the second set of operands from either the third primary or the third secondary registers (paragraph 0026; FIG. 2).

Appellants' Claim 27 provides: wherein the primary calculating unit is controlled by the opcode to perform a first operation on the first set of operands and the secondary calculating unit is controlled by the opcode to perform a second operation on the second set of operands (see paragraph 0026; FIG. 2).

Appellants' Claim 28 also provides: wherein the first operation differs from the second operation (paragraph 0026; FIG. 2).

Appellants' Claim 29 provides: wherein the first and second operations both include multiplying their respective first and third operands to obtain respective first products and adding or subtracting their respective second operands to or from the respective first products (paragraph 0027; FIG. 4).

Appellants' Claim 30 further provides: wherein the first, second, and third operands of the first and second sets of operands are all floating point formatted operands (paragraph 0018, 0019, 0026; FIG. 2).

Appellants' Claim 31 provides: [a] microprocessor (100) including: an execution unit 200 enabled to execute an asymmetric instruction 300, wherein the asymmetric instruction 300 includes a set of three operand register fields (306, 308, 310) and a target register field and an operation code (opcode) 302-1, 302-2 (see paragraphs 0024, 0026; FIG. 2, FIG. 3); a register file 201 accessible by the execution unit 200 and having a rank of two including a primary register file 202 and a secondary register file 203 wherein a value in an operand register field identifies a register in the primary register file 202 and a corresponding register in the secondary register file 204 (paragraph 0023, 0026, 0027; FIG. 2); wherein the execution unit 200 is configured to perform a first operation on a first set of three operands selected from registers identified by the set of operand register fields and to perform a second operation on a second set of three operands also selected from the registers identified by the set of operand registers fields wherein the first and second operations and selection of the first and second sets of operands are determined by the opcode 302-1, 302-2 (see paragraph 0024, 0025; FIG. 2, FIG. 3).

Appellants' Claim 32 further provides: wherein at least one condition selected from a group of conditions consisting of the first and second operations being different and the first and second sets of operands being different is true (paragraph 0017, FIG. 2).

Appellants' Claim 33 provides: wherein the execution unit is further configured to store a result of the first operation in a register of the primary register file determined by the target register field and the result of the second operation in a register of the secondary register field also determined by the target register field (see paragraph 0022, FIG. 2).

Appellants' Claim 34 further provides: including multiplexing circuitry controlled by the opcode to select a first of the first set of three operands from a first primary and a first secondary register identified by a first operand register field, a second of the first set of three operands from

a second primary and a second secondary register identified by a second operand register field, a third of the first set of three operands from a third primary and a third secondary register identified by a first operand register field, a first of the second set of three operands from a first primary and a first secondary register identified by a first operand register field, a second of the second set of three operands from a second primary and a second secondary register identified by a second operand register field, and a third of the second set of three operands from a third primary and a third secondary register identified by a first operand register field (paragraph 0024; FIG. 2; FIG. 3).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. The Examiner's rejection of Claims 1, 4, 7-9 and 21-34 under 35 U.S.C. §103(a) as being anticipated by *Wang et al.* (U.S. Patent No. 5,187,796) in view of *Matsuo* (U.S. Patent No. 5,901,301) and further in view of *Sih* (U.S. Patent No. 6,557,022) is to be reviewed on Appeal.

ARGUMENT

A. The rejection of Claims 1, 4, 7-9 and 21-34 under 35 U.S.C. §103(a) as being anticipated by *Wang et al.* in view of *Matsuo* and further in view of *Sih* is not well founded and should be reversed.

1. General requirements for a claim rejection under 35 U.S.C. § 103

According to 35 U.S.C. §103(a):

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Examiner improperly rejects Claims 1, 4, 7-9 and 21-34 as being unpatentable over *Wang* in view of *Matsuo* and further in view of *Sih* under 35 USC §103. The combination of references does not render Appellants' claimed invention unpatentable because that combination does not render obvious, to one skilled in the art at the time of Appellants' invention, several of the features recited by Appellants' claims. For example, the combination fails to render obvious the following features (among others) of Appellants' Claims 1, 4, 9, 25, and 31:

(a) a vector unit to execute a vector instruction to perform a first operation on a first set of three operands and a second operation on a second set of three operands, said vector unit configured with three inputs, one for each of the three operands, which are received at the vector unit at substantially a same time.

(b) wherein the vector unit includes a 3-input primary unit and a 3-input secondary unit, wherein the primary unit is configured to perform the first operation on the first set of operands and the 3-input secondary unit is configured to perform the second operation on the second set of operands.

(c) wherein the vector register file contains information representing a real portion of a complex number in the primary register file and an imaginary portion of the complex number in the secondary register file.

On page 4 of the Office Action, in explaining the motivation to combine *Matsuo* in view of *Wang*, the Examiner states "[i]t would have been obvious to one of ordinary skill in the art at the time of invention to have included *Matsuo's* method of adding a third operand to the product of first and second operands in Wang's invention for the benefit of higher speed processing". To establish a prima facie case of obviousness, one of the three basic criteria requires the prior art reference (or references when combined) teach or suggest all the claim limitations. *Matsuo* in view of *Wang*, in further view of *Sih* fail to teach all the claim limitations..

Neither *Matsuo* nor *Wang* suggest the use of a vector unit as taught within the Appellants' claimed invention, nor could anyone of ordinary skill in the art modify *Matsuo* or *Wang* to render Appellants' claimed invention. With respect to the references, the Examiner admits "*Wang* fails to disclose 3-input execution units" (Office Action, page 3); However, the Examiner improperly proposes that *Matsuo* discloses a 3-input primary floating point unit. Column 27, lines 47-52 of *Matsuo*, relied on by the Examiner, generally provides a 3-operand

instruction that is a multiply-add operand. A closer read of *Matsuo* clearly indicate that the operations are not processed at "substantially the same time", and the teachings of *Matsuo* are void of executing "a vector instruction to perform a first operation on a first set of three operands and a second operation on a second set of three operands", as presented by Appellants' independent claims.

Matsuo clearly does not teach 3-input execution, despite the Examiner's unsubstantiated and clearly inaccurate suggestions that Appellants' "3-input execution unit" and *Matsuo's* "3-operand instruction" (*Matsuo,* Column 27, lines 47-50) are/may be synonymous. A "3-operand instruction" is not capable of performing "a first operation on a first set of three operands and a second operation on a second set of three operands, said vector unit configured with three inputs, one for each of the three operands, which are received at the vector unit at substantially a same time," and therefore that element of Appellants' claims is not taught by *Matsuo*.

The Examiner clearly mischaracterizes the 3-operand instruction presented by *Matsuo*. The Examiner has also failed to recognize that the 3-operand instruction presented by *Matsuo* merely enables a first register value and a second register value to be multiplied and the result of multiplication added to the value in the pair of register (*see Matsuo*, Column 27, lines 47-52). The 3-operand instruction, as presented by *Matsuo*, is incapable of executing a vector instruction to perform multiple operations on a set of 3-operands, as taught within the Appellants' claimed invention.

As clear evidence of the Examiner's misrepresentation of *Matsuo*, the Examiner fails to accurately compare the features of *Matsuo's* 3-operand instruction against Appellants' "vector unit configured with three inputs". The Examiner further admits that *Wang* does not disclose the "3-input execution unit". Thus, *Matsuo* does not teach or suggest, individually or in combination with *Wang*, the vector instruction to perform the multiple operands at substantially the same time (via a vector unit configured with three inputs), as presented by Appellants' claimed invention. Therefore, the Examiner has failed to establish a prima facie case of obviousness with respect to at least this important element of Appellants' claim.

Sih also does not disclose the "3-input execution unit". On page 4 of the Office Action, the Examiner relies on *Sih*, (FIG. 2, Column 3, lines 13-30) to support a notion that *Sih* discloses a vector unit that receives three operands at substantially the same time. The Examiner states "*Sih* discloses a [multiply-accumulate] MAC unit that contains enough output ports to the

register file to allow the MAC unit to receive all its inputs at the same time." However, a careful examination of *Sih* by Appellants confirms that *Sih* neither teaches nor suggest the "3-input execution unit". Contrary to the Examiners proposed notion, *Sih* presents no support for receiving the three operands at substantially the same time via a vector unit configured with three inputs. The Examiner's assumption that the MAC unit provided by *Sih* has enough output ports to allow the inputs to be received at the same time is invalid because the bit capacity provided by *Sih* is not capable of performing the complex arithmetic applications provided within the Appellants' claimed invention.

Additionally, the functionality of the Appellants' claimed invention is destroyed when *Matsuo*, *Wang*, and *Sih* are combined. More specifically, the combination is incapable of executing the vector register file when the "vector register file contains information representing a real portion of a complex number in the primary register file and an imaginary portion of the complex number in the secondary register file," as presented by the Appellants' claimed invention. Thus, the combination of *Sih* with *Matsuo* and *Wang* fails to render the Appellants' claimed element obvious, and Examiner again fails to meet the criteria for establishing aprima facie case of obviousness.

The Examiner has mischaracterized the references and/or the specific features of Appellants' Claims 1, 4, 9, 25, and 31 which features demonstrate the novelty of Appellants' claimed invention, and which features are not taught or suggested by none of *Matsuo*, *Wang*, nor *Sih*. Accordingly, the Examiner has failed to meet at least one criterion required to establish a prima facie case of obviousness, which criterion requires that the prior art references must teach or suggest all the claim limitations.

From the above discussion/arguments and the reasons provided therein, it is clear that the combination of references does not render obvious key features of Appellants' claimed invention. One skilled in the art would not find Appellants' claimed invention unpatentable over the combination of references. The rejection of Claims 1, 4, 7-9 and 21-34 for the above reasons, is not well founded and should be reversed.

B. The rejection of Claim 10 under 35 U.S.C. 103(a) as being unpatentable over *Wang* in view of *Matsuo* in view of *Sih* in further view of *Golliver et al.* (U.S. Pub. No. US 2002/0004809) are not well founded and should be reversed.

Claim 10, which recites "the vector unit is configured to execute a complex computation instruction in which the imaginary portion of the first operand of the first set of operands is multiplied by an imaginary portion of a second operand in the first operation and in which the imaginary portion of the first operand is multiplied by a real portion of the second operand in the second operation," is rejected by the Examiner. The Examiner admits *Wang* and *Matsuo* fails to disclose "wherein the vector is configured to perform a complex operation…in the second operation" of Appellants' Claim 10. The Examiner mistakenly states that *Golliver* discloses "a vector unit configured to perform a complex operation…"(Office Action, page 2, section 11). The Examiner relies on AiBr of FIG. 3A to support the assumption that *Golliver* discloses "a vector unit configured to perform a complex operation…" The Examiner overlooks or fails to recognize the complex and imaginary numbers (see *Golliver* paragraph 0026) which "packed data item" (350, of FIG. 3A) participate in a multiply-add instruction with two other packed data items. "AiBr" as relied on by the Examiner, is not executed via a vector unit. Additionally, neither *Wang*, *Matsuo*, nor *Sih* teach or suggest the "vector unit" as presented by the Appellants' claimed invention.

Moreover, Claim 10 depends on independent Claim 1, which Appellants have shown by the above arguments to be allowable over the combination of references. By the dependence of Claim 10 on an allowable base Claim 1, the present dependent claim is therefore also allowable. The rejection of Appellant's Claim 10 is thus not well founded and should be reversed.

CONCLUSION

Appellants have pointed out with specificity the manifest error in the Examiner's rejections and the claim language which renders the invention patentable over the various combinations of references. Appellants, therefore, respectfully request that this case be remanded to the Examiner with instructions to issue a Notice of Allowance for all pending claims.

Respectfully submitted,

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APPENDIX

1. A microprocessor, comprising:

a vector unit to execute a vector instruction to perform a first operation on a first set of three operands and a second operation on a second set of three operands, said vector unit configured with three inputs, one for each of the three operands, which are received at the vector unit at substantially a same time;

a vector register file having a primary register file and a secondary register file, each having a first register, a second register and a third register with the operands provided therein;

wherein the vector instruction includes a first register field indicative of a first primary register in the primary register file and a first secondary register in the secondary register file, a second register field indicative of a second primary register in the primary register file and a second secondary register in the secondary register file, and a third register field indicative of a third primary register in the primary register file and a third secondary register in the secondary register file; and

wherein the first set of operands includes a first operand selected from the first primary register or the first secondary register, a second operand selected from the second primary register or the second secondary register, and a third operand selected from the third primary register or the third secondary register, wherein the selection of the operands occurs at substantially a same time to provide an input of the three operands to the vector unit via the three inputs.

2-3. (canceled)

4. The microprocessor of claim 1, wherein the vector unit includes a 3-input primary unit and a 3-input secondary unit, wherein the primary unit is configured to perform the first operation on the first set of operands and the 3-input secondary unit is configured to perform the second operation on the second set of operands.

5-6. (canceled)

7. The microprocessor of claim 1, wherein the first and second operations use at least one operand from the primary register file and at least one operand from the secondary register file.

8. The microprocessor of claim 1, wherein the first and second sets of operands include at least one common operand.

9. The microprocessor of claim 1, wherein the vector register file contains information representing a real portion of a complex number in the primary register file and an imaginary portion of the complex number in the secondary register file.

10. The microprocessor of claim 9, wherein the vector unit is configured to execute a complex computation instruction in which the imaginary portion of the first operand of the first set of operands is multiplied by an imaginary portion of a second operand in the first operation and in which the imaginary portion of the first operand is multiplied by a real portion of the second operand in the second operation.

11-20. (canceled)

21. The microprocessor of claim 1, wherein the second set of operands include a first operand selected from the first primary register or the first secondary register, a second operand selected from the second primary register or the second secondary register, and a third operand selected from the third primary register or the third secondary register.

22. The microprocessor of claim 4, wherein the first operation includes multiplying two of the three first set of operands to obtain a first product and adding or subtracting the remaining of the first set of operands to or from the first product and wherein the second operation includes multiplying two of the three second set of operands to obtain a second product and adding or subtracting the remaining of the second set of operands to or from the second product.

23. The microprocessor of claim 22, wherein the first and second sets of operands comprise first and second sets of floating point formatted operands.

24. The microprocessor of claim 1, wherein the vector instruction includes a target register field indicative of a primary target register in the primary register file and a secondary target register in the secondary register file and further wherein the vector unit is further configured to store a result of the first operation in the primary target register and to store a result of the second operation in the secondary target register.

25. A vector unit to process a vector instruction having an opcode and first, second, and third register fields, comprising:

a register file including a primary register file having a set of primary registers and a secondary register file having a set of secondary registers, wherein each register field identifies a register in the primary register file and a corresponding register in the secondary register file, wherein the set of primary registers and set of secondary registers each have a first register, a second register and a third register with operands provided therein;

primary and secondary calculating units, wherein the primary calculating unit includes first, second, and third inputs to receive, respectively, first, second, and third operands of a first set of operands and wherein the secondary calculating unit includes first, second, and third inputs to receive, respectively, first, second, and third operands of a second set of operands;

wherein the first set of operands includes a first operand selected from the first primary register or the first secondary register, a second operand selected from the second primary register or the second secondary register, and a third operand selected from the third primary register or the third secondary register, wherein the selection of the operands occurs at substantially a same time to provide an input of the three operands to the vector unit via the three inputs;

wherein the three operands are received at the vector unit from the register files at substantially a same time; and

multiplexing circuitry controlled by the opcode to select each of the first, second, and third operands in the first and second set of operands from the set of primary and secondary file registers identified by the register fields.

26. The vector unit of claim 25, wherein the multiplexing circuitry is controlled by the opcode to select:

the first operand in the first set of operands from either the first primary or the first secondary registers;

the second operand in the first set of operands from either the second primary or the second secondary registers; and

the third operand in the first set of operands from either the third primary or the third secondary registers;

the first operand in the second set of operands from either the first primary or the first secondary registers,

the second operand in the second set of operands from either the second primary. or the second secondary registers; and

the third operand in the second set of operands from either the third primary or the third secondary registers

27. The vector unit of claim 25, wherein the primary calculating unit is controlled by the opcode to perform a first operation on the first set of operands and the secondary calculating unit is controlled by the opcode to perform a second operation on the second set of operands.

28. The vector unit of claim 27, wherein the first operation differs from the second operation.

29. The vector unit of claim 27, wherein the first and second operations both include multiplying their respective first and third operands to obtain respective first products and adding or subtracting their respective second operands to or from the respective first products.

30. The vector unit of claim 25, wherein the first, second, and third operands of the first and second sets of operands are all floating point formatted operands.

31. A microprocessor including:

an execution unit enabled to execute an asymmetric instruction, wherein the asymmetric instruction includes a set of three operand register fields and a target register field and an operation code (opcode);

a register file accessible by the execution unit and having a rank of two including a primary register file and a secondary register file wherein a value in an operand register field identifies a register in the primary register file and a corresponding register in the secondary register file, wherein the set of primary registers and set of secondary registers each have a first register, a second register and a third register with operands provided therein;

wherein the execution unit is configured to perform a first operation on a first set of three operands selected from registers identified by the set of operand register fields and to perform a second operation on a second set of three operands also selected from the registers identified by the set of operand registers fields wherein the first and second operations and selection of the first and second sets of operands are determined by the opcode;

wherein the first set of operands includes a first operand selected from the first primary register or the first secondary register, a second operand selected from the second primary register or the second secondary register, and a third operand selected from the third primary register or the third secondary register, wherein the selection of the operands occurs at substantially a same time to provide an input of the three operands to the vector unit via the three inputs; and

wherein the three operands are received from the register files at substantially a same time.

32. The microprocessor of claim 31, wherein at least one condition selected from a group of conditions consisting of the first and second operations being different and the first and second sets of operands being different is true.

33. The microprocessor of claim 31, wherein the execution unit is further configured to store a result of the first operation in a register of the primary register file determined by the target register field and the result of the second operation in a register of the secondary register field also determined by the target register field.

34. The microprocessor of claim 31, including multiplexing circuitry controlled by the opcode to select a first of the first set of three operands from a first primary and a first secondary register identified by a first operand register field, a second of the first set of three operands from

a second primary and a second secondary register identified by a second operand register field, a third of the first set of three operands from a third primary and a third secondary register identified by a first operand register field, a first of the second set of three operands from a first primary and a first secondary register identified by a first operand register field, a second of the second set of three operands from a second primary and a second secondary register identified by a second operand register field, and a third of the second set of three operands from a third primary and a third secondary register identified by a first operand register field.

EVIDENCE APPENDIX

Other than the Office Action(s) and reply(ies) already of record, no additional evidence has been entered by Appellants or the Examiner in the above-identified application which is relevant to this appeal.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings as described by 37 C.F.R. §41.37(c)(1)(x) known to Appellants, Appellants' legal representative, or assignee.